Electronic Version
Stylesheet Version v1.1.1

FREQUENCY DIVIDER AND RELATED METHOD OF DESIGN

Abstract

A frequency divider and related frequency divider designing method for forming a target clock by dividing an original clock by n.5 are disclosed. The method includes the following steps: (a) determining a frequency-dividing ratio of n.5*2, (b) generating a first triggering phase and a second triggering phase relating to the original clock by determining the frequency-dividing ratio, (c) selecting a positive frequency dividing circuit or a negative frequency dividing circuit and an initial value setting manner for the selected positive or negative frequency dividing circuits, and (d) generating the target clock according to the first and second target clocks.